IN THE SPECIFICATION

Please replace the paragraph beginning at page 35, line 24 with the following regarding written paragraphs.

3T1D memory cell 1900 comprises one or more bitlines 1905, a ground 1910, two ground metal contacts 1911 and 1912, with a global ground line running every two cells to every 16 cells in parallel with the bitlines (in the figure, a ground line is shown behind a bitline), a read bitline (BLr) 1915 and its metal contacts 1916 and 1917, a write wordline (WLw) 1920 and its metal contact 1921, a write bitline (BLw) 1925 and its metal contacts 1926 and 1927, a drain diffusion area 1975, a gate 1978, a gate insulator 1983, a source diffusion area 1970, an MCBar metal contact 1991, a Shallow Trench Isolation (STI) region 1965, a polysilicon gate 1994, a read wordline (WLr) 1945 with metal contacts 1933 and 1940, STI regions 1950 and 1953, a p-well 1992, an optional n-isolation band 1955, a p-substrate 1960 and an insulating layer 1930. The gated diode 1904 is formed from the gate ~~1904~~ 1994 and the gate insulator 1990 and a source (not shown). The source of the gated diode 1904 is coupled to the WLr 1945 through metal contact 1933. The portion 1992 separates gate insulator 1990 and gate insulator 1993. Typically, the portion 1992 would be filled with polysilicon from the gate 1994.

The write FET 1901 is formed by gate 1978, gate insulator 1983, and source/drain diffusion areas 1970, 1975, and is connected to the WLw line 1920 through metal contact 1921. The read select FET 1902 is formed in front of the gate 1994, while the read FET 1903 is formed behind the gate 1994. The source (not shown) of the read select FET 1902 is connected to the drain (not shown) of the read FET 1903 (shown behind the gate 1994). The drain (not shown) of the read select FET 1902 is in front of the gate ~~1904~~ 1994 and the FET channel (not shown) for the read select FET 1902 is into the page. The source (not shown) of the read FET 1903 is connected to the GND line 1910 (behind the gate 1994) and through metal contact 1912. The gate (not shown) of the read FET 1903 is behind the gate 1994 and the FET channel (not shown) is into the page. The MCBar 1991 connects the source diffusion area 1970 to the gate of the read FET 1903. The gate 1983, gate 1994, and the gates (not shown) for the read FET 1903 and the read select FET are typically made of polysilicon that has been highly doped (e.g., N+). In this example, the writeline WLr 1933 and control line WLrs 1940 have been combined.